

Notice of Allowability	Application No.	Applicant(s)
	10/730,120	SHIBATA, KOHSAKU
	Examiner Kandasamy Thangavelu	Art Unit 2123

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. This communication is responsive to 10 May 2007.
2. The allowed claim(s) is/are 1-23.
3. Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) All
 - b) Some*
 - c) None
 of the:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
5. CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
 - (a) including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
 - 1) hereto or 2) to Paper No./Mail Date _____.
 - (b) including changes required by the attached Examiner's Amendment / Comment or in the Office action of
 Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. Notice of References Cited (PTO-892)
2. Notice of Draftsperson's Patent Drawing Review (PTO-948)
3. Information Disclosure Statements (PTO/SB/08),
Paper No./Mail Date _____
4. Examiner's Comment Regarding Requirement for Deposit
of Biological Material
5. Notice of Informal Patent Application
6. Interview Summary (PTO-413),
Paper No./Mail Date _____.
7. Examiner's Amendment/Comment
8. Examiner's Statement of Reasons for Allowance
9. Other Clean copy of Allowed Claims.

DETAILED ACTION

Introduction

1. This communication is in response to the Applicants' communication dated May 10, 2007. Claims 1, 22 and 23 were amended. Claims 1-23 of the application are pending.

Examiner's Amendment

2. Authorization for this examiner's amendment was given in a telephone conversation by Mr. Andrew Dunlap on June 25, 2007.

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to the applicants, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

3. In the claims:

Claim 1, Lines 3-5, "a first simulation unit configured to simulate, in the same stage in pipeline processing, execution of a group of instructions intended to be simultaneously executed, and to generate a first simulation result"

has been changed to

--a first simulation unit configured to simulate execution of a group of instructions on a cycle-by-cycle basis, said group of instructions comprising instructions in the same stage of pipeline processing and said instructions being intended to be simultaneously executed and being simulated successively, and to generate a first simulation result--.

Claim 11, Lines 5-6, "the simulation of the instruction of said group of instructions"

has been changed to

-- the simulation of said group of instructions --.

Claim 22, Lines 3-5, "performing a first simulation comprising simulating, in the same stage in pipeline processing, execution of a group of instructions comprising a plurality of instructions intended to be simultaneously executed, and generating a first simulation result of said first simulation"

has been changed to

--performing a first simulation comprising simulating execution of a group of instructions on a cycle-by-cycle basis, said group of instructions comprising instructions in the same stage of pipeline processing and said instructions being intended to be simultaneously executed and being simulated successively, and generating a first simulation result of said first simulation--.

Claim 23, Lines 4-6, "performing a first simulation comprising simulating, in the same stage in pipeline processing, execution of a group of instructions comprising a plurality of

instructions intended to be simultaneously executed, and generating a first simulation result of said first simulation”

has been changed to

--performing a first simulation comprising simulating execution of a group of instructions on a cycle-by-cycle basis, said group of instructions comprising instructions in the same stage of pipeline processing and said instructions being intended to be simultaneously executed and being simulated successively, and generating a first simulation result of said first simulation--.

A clean copy of allowed claims is attached.

Reasons for Allowance

4. Claims 1-23 of the application are allowed over prior art of record.
5. The following is an Examiner's statement of reasons for the indication of allowable subject matter:

The closest prior art of record shows:

(1) simulating the behavior of multi-parallel-stage Very long instruction word (VLIW) processors; since the simulator is run on an existing processor to emulate the design of the VLIW processor, the simulator performs sequentially a large number of internal operations which will be done in parallel in the VLIW processor; the operation of a single instruction is done in a number of stages using fetch, decode, execute and post stages in a pipeline; the execution of a

single instruction takes multiple cycles; all stages may be in use simultaneously each performing tasks associated with different instructions; the simulation process computes and stores within each simulated pipeline stage, a large amount of information needed by subsequent stage; in VLIW architecture, parallel pipelines exist, one pipeline for each execution unit which execute simultaneously; the method significantly increases the performance of the simulator by substantially reducing the storing and copying of redundant information; this is achieved by reordering the chronological sequence of execution of software models of the various pipeline stages, taking advantage of the independence of the stages and independence of the execution units (**Moller et al.**, U.S. Patent 6,826,522);

(2) instruction level parallelism (ILP) is the ability to execute several operations simultaneously; processors capable of exploiting ILP contain multiple execution units, fetch several instructions per cycle from the instruction cache and in a given cycle may dispatch multiple operations for execution; such processors are called superscalar processors or very long instruction word (VLIW) processors; the VLIW processor constructs a parallelized long instruction sequence at compile time; the VLIW processor can be implemented using simpler hardware units, but the object code is more complex, since it contains groups of long instructions, each of which is composed of a number of instructions; the compressed VLIW processor (CVLIW) individually schedules each instruction in the long instructions using a number of functional unit and individual scheduler pairs; each scheduler individually decides to issue next instruction to its functional unit or stall the functional unit for next pipeline cycle due to resource collision or data dependencies; analyzing the performance of the CVLIW processor

using a simulator; the simulator compiles a C language application and generates MIPS assembly code; the assembly code is passed to three parallelizers, each associated with a unique processor; the parallelizers generate parallelized code for the processor simulator and generate object code; the simulators use the object code and compute the total number of execution cycles required for execution; the performance of the CVLIW processor is calculated by comparing the three processor's total number of execution cycles; the CVLIW's performance is 9% to 15% higher than that of the VLIW processor (**Jee et al.**, "Performance evaluation of for a compressed VLIW processor", ACM, March, 2002); and

(3) a method of generating a system LSI design and development environment; the method comprises analyzing an input command, generating a compiler customization section, an assembler customizing section and a simulator generation section on the basis of information from a configuration designation file; the simulator has means for outputting an execution result of a debug command when a specific address is passed; an assertion error program outputs an error when an error has occurred; to check the progress when a device is normally executing, an instruction for outputting an intermediate result is embedded in the application or the execution is stopped by the debugger to read the progress; when memory access to an undesignated area occurs, the simulator stops execution and issues a warning; when the simulator is executing in an interactive mode, the simulator interrupts simulation operation to analyze the position of the error and displays access error to an invalid area; a program can be generated in a high level language and the performance of the program evaluated using the VLIW simulator (**Matsumoto et al.**, U.S. Patent Application 2003/0204819).

Additional state of the art reviewed and considered by the Examiner is found in U.S. Patent 7,051,309; U.S. Patent 6,871,298; U.S. Patent 6,397,324; Sami et al., "An instruction level energy model for embedded VLIW architectures" IEEE, September 2002; Jouppi et al., "Available instruction level parallelism for superscalar and superpipelined machines", ACM 1989.

None of these references taken either alone or in combination with the prior art of record discloses a simulation apparatus for simulating a very long instruction word processor, specifically including:

(Claim 1) "a first simulation unit configured to simulate execution of a group of instructions on a cycle-by-cycle basis, said group of instructions comprising instructions in the same stage of pipeline processing and said instructions being intended to be simultaneously executed and being simulated successively, and to generate a first simulation result; and

 a second simulation unit configured to simulate, based on the first simulation result generated by said first simulation unit, a sequential execution of said group of instructions on an instruction-by-instruction basis and to generate a second simulation result".

None of these references taken either alone or in combination with the prior art of record discloses a simulation method for simulating a very long instruction word processor, specifically including:

(Claim 22) "performing a first simulation comprising simulating execution of a group of instructions on a cycle-by-cycle basis, said group of instructions comprising instructions in the same stage of pipeline processing and said instructions being intended to be simultaneously executed and being simulated successively, and generating a first simulation result of said first simulation; and

performing a second simulation comprising simulating, based on the first simulation result, a sequential execution of said group of instructions on an instruction-by-instruction basis and generating a second simulation result of said second simulation".

None of these references taken either alone or in combination with the prior art of record discloses a computer-readable recording medium which stores a program for executing on a computer a simulation of a very long instruction word processor, specifically including:

(Claim 23) "performing a first simulation comprising simulating execution of a group of instructions on a cycle-by-cycle basis, said group of instructions comprising instructions in the same stage of pipeline processing and said instructions being intended to be simultaneously executed and being simulated successively, and generating a first simulation result of said first simulation; and

performing a second simulation comprising simulating, based on the first simulation result, a sequential execution of said group of instructions on an instruction-by-instruction basis and generating a second simulation result of said second simulation".

6. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Kandasamy Thangavelu whose telephone number is 571-272-3717. The examiner can normally be reached on Monday through Friday from 8:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul Rodriguez, can be reached on 571-272-3753. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to TC 2100 Group receptionist: 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



K. Thangavelu
Art Unit 2123
June 25, 2007

Clean Copy of Allowed claims

1. A simulation apparatus for simulating a very long instruction word processor, said simulation apparatus comprising:

a first simulation unit configured to simulate execution of a group of instructions on a cycle-by-cycle basis, said group of instructions comprising instructions in the same stage of pipeline processing and said instructions being intended to be simultaneously executed and being simulated successively, and to generate a first simulation result; and

a second simulation unit configured to simulate, based on the first simulation result generated by said first simulation unit, a sequential execution of said group of instructions on an instruction-by-instruction basis and to generate a second simulation result.

2. The simulation apparatus according to Claim 1, wherein said second simulation unit is configured to generate the second simulation result by undoing the simulation of the execution of one of the instructions from said group of instructions previously simulated by said first simulation unit.

3. The simulation apparatus according to Claim 2 further comprising a display control unit configured to control a display unit to display the second simulation result generated by said second simulation unit.

4. The simulation apparatus according to Claim 2, wherein said second simulation unit includes:

a judgment unit configured to judge whether or not an instruction that satisfies a break condition is included in the execution of said group of instructions previously simulated by said first simulation unit;

an indication unit configured to direct said first simulation unit to simulate execution of a next group of instructions when said judgment unit judges that no instruction satisfying the break condition is included in the execution of said group of instructions previously simulated by said first simulation unit;

a determination unit configured to determine that an instruction of said group of instructions is a stop instruction when said judgment unit judges that the instruction satisfying the break condition is included; and

a generation unit configured to generate a simulation result by undoing simulations of the execution of the stop instruction and subsequent instructions in the execution of said group of instructions previously simulated.

5. The simulation apparatus according to Claim 1, wherein
said first simulation unit is configured to simulate a pipeline processor that
simultaneously executes a plurality of instructions, and
said simulation apparatus further comprises a display image generation unit
configured to generate a display image showing instructions included in a pipeline based on
the first simulation results generated by said first simulation unit and the second simulation
results generated by said second simulation unit.

6. The simulation apparatus according to Claim 5, wherein the display image contains a representation of an instruction included in every stage of the pipeline.

7. The simulation apparatus according to Claim 1, wherein said first simulation unit is configured to simulate, on a cycle-by-cycle basis, a pipeline processor that simultaneously executes a plurality of instructions, said simulation apparatus further comprises:

an acception unit configured to accept a user instruction for indicating a step to be executed on the instruction-by-instruction basis and for indicating a step to be executed on the cycle-by-cycle basis; and

a display image generation unit configured to generate a display image showing the second simulation result generated by said second simulation unit when the user instruction that indicates the step to be executed on the instruction-by-instruction basis is accepted by said acception unit, and to generate a display image showing a simulation result generated on the cycle-by-cycle basis by said first simulation unit when the user instruction that indicates the step to be executed on the cycle-by-cycle basis is accepted by said acception unit.

8. The simulation apparatus according to Claim 7, wherein the display image contains a representation of each instruction included in the pipeline.

9. The simulation apparatus according to Claim 7, wherein the display image contains a representation of each instruction included in every stage of the pipeline.

10. The simulation apparatus according to Claim 1, wherein said first simulation unit includes:

a hold unit configured to hold first data indicating resources of the very long instruction word processor;

a storage unit configured to store a copy of the first data in a memory unit as second data; and

a first simulator configured to update the first data by simulating an execution of a single group of instructions after said storage unit stores the copy of the first data, wherein said second simulation unit is configured to obtain the second simulation results of the execution of said group of instructions on the instruction-by-instruction basis based on the first data and the second data.

11. The simulation apparatus according to Claim 10, wherein said storage unit is configured to store register data in the memory unit as the second data, and

said second simulation unit is configured to reconstruct data indicating a resource of the very long instruction word processor before executing the simulation of said group of instructions on the instruction-by-instruction basis.

12. The simulation apparatus according to Claim 11, wherein said storage unit is configured to store memory data before memory writing, in said hold unit, and to store the memory data so that the memory data is contained in the second data when a memory write instruction is included in said group of instructions.

13. The simulation apparatus according to Claim 10, wherein said second simulation unit further comprises:

a judgment unit configured to judge whether or not an instruction that satisfies a break condition is included in the execution of said group of instructions previously simulated by said first simulation unit;

an indication unit configured to direct said first simulation unit to simulate execution of a next group of instructions when said judgment unit judges that no instruction satisfying the break condition is included in the execution of said group of instructions previously simulated by said first simulation unit; and

a determination unit configured to determine that an instruction is a stop instruction when said judgment unit judges that the instruction satisfying the break condition is included.

14. The simulation apparatus according to Claim 13, wherein said determination unit is configured to determine that an instruction next to a present stop instruction is a break condition in a step of execution of a simulation performed on an instruction-by-instruction basis.

15. The simulation apparatus according to Claim 13, wherein said second simulation unit further comprises a reconstruction unit configured to reconstruct, based on the first data and the second data, data indicating the resources of the very long instruction word processor, on a condition that execution of previous instructions, up to an instruction just prior to the stop instruction determined by said determination unit, has been simulated.

16. The simulation apparatus according to Claim 13, wherein said second simulation unit further comprises a reconstruction unit configured to reconstruct, based on the first data and the second data, data indicating the resources of the very long instruction word processor, on a condition that execution of previous instructions, up to the stop instruction determined by said determination unit, has been simulated.

17. The simulation apparatus according to Claim 16, wherein said first simulator is configured to generate update information indicating resources of the very long instruction word processor to be changed by each instruction of said group of instructions, and

 said reconstruction unit is configured to reconstruct the data from the resources of the very long instruction word processor that correspond to a result of a sequential execution of the instructions of said group of instructions according to the first data, the second data, and the update information.

18. The simulation apparatus according to Claim 10, wherein said first simulator is configured to simulate an execution of the group of instructions on a cycle-by-cycle basis of pipeline processing, and the simulation apparatus is configured to count a quantity of execution cycles in the simulation for every group of instructions.

19. The simulation apparatus according to Claim 18, wherein

the very long instruction word processor to be simulated includes a cancellation unit configured to cancel an execution of an instruction within a plurality of instructions to be simultaneously executed, and

 said first simulator is configured to simulate said cancellation unit.

20. The simulation apparatus according to Claim 18, wherein
 said first simulator is configured to simulate a delay cycle according to a delay instruction that causes a delay cycle in an execution stage of the very long instruction word processor to be simulated, and

 said reconstruction unit is configured to reconstruct data indicating the resources of the very long instruction word processor that correspond to a simulation result from simulating the delay cycle according to update information for the delay instruction.

21. The simulation apparatus according to Claim 20, wherein said reconstruction unit is configured to generate data indicating the resources of the very long instruction word processor that correspond to a simulation result of simulating an output dependency instruction according to the update information for the delay instruction and according to the update information for the output dependency instruction that has an output dependency in the same group of instructions as the delay instruction.

22. A simulation method for simulating a very long instruction word processor, said simulation method comprising:

performing a first simulation comprising simulating execution of a group of instructions on a cycle-by-cycle basis, said group of instructions comprising instructions in the same stage of pipeline processing and said instructions being intended to be simultaneously executed and being simulated successively, and generating a first simulation result of said first simulation; and

performing a second simulation comprising simulating, based on the first simulation result, a sequential execution of said group of instructions on an instruction-by-instruction basis and generating a second simulation result of said second simulation.

23. A computer-readable recording medium which stores a program for executing on a computer a simulation of a very long instruction word processor, the program causing the computer to execute a method comprising:

performing a first simulation comprising simulating execution of a group of instructions on a cycle-by-cycle basis, said group of instructions comprising instructions in the same stage of pipeline processing and said instructions being intended to be simultaneously executed and being simulated successively, and generating a first simulation result of said first simulation; and

performing a second simulation comprising simulating, based on the first simulation result, a sequential execution of said group of instructions on an instruction-by-instruction basis and generating a second simulation result of said second simulation.